Joint
Transportation
Research
Program

JTRP

FHWA/IN/JTRP-98/3

Final Report

Borman Expressway Point-to-Point Wireless Modem

James V. Krogmeier
Michael P. Fitz

June 2000

Indiana
Department
of Transportation

Purdue
University

Final Report

FHWA/IN/JTRP-98/03

Borman Expressway Point-to-Point Wireless Modem

By

J. V. Krogmeier
School of Electrical and Computer Engineering
Purdue University

Joint Transportation Research Program
Project No. C-36-75H
File No. 8-9-8
SPR-2036

In Cooperation with the
Indiana Department of Transportation
and the
U.S. Department of Transportation
Federal Highway Administration

Purdue University
West Lafayette, Indiana 47907
June 2000

TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
FHWA/IN/JTRP-98/13		

4. Title and Subtitle	5. Report Date
Borman Expressway Point-to-Point Wireless Modem	June 2000
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
James V. Krogmeier and Michael P. Fitz	FHWA/IN/JTRP-98/3

9. Performing Organization Name and Address	10. Work Unit No.
Joint Transportation Research Program 1284 Civil Engineering Building Purdue University West Lafavette. Indiana 47907-1284	
	11. Contract or Grant No. SPR-2036

12. Sponsoring Agency Name and Address	13. Type of Report and Period Covered
Indiana Department of Transportation State Office Building 100 North Senate Avenue Indianapolis, IN 46204	Final Report
	14. Sponsoring Agency Code

15. Supplementary Notes

Prepared in cooperation with the Indiana Department of Transportation and Federal Highway Administration.

16. Abstract

The Federal Highway Administration has a nationwide allocation of five frequency pairs in the 220-222 MHz Narrowband Radio Services band which are intended for application in Intelligent Transportation Systems. These frequencies are available for use by state DOTs (subject to FHWA approval) and provide an attractive solution for certain low to medium bit rate data communications applications. However, given the limited bandwidth available in these channels, very efficient modems will be required to make maximum beneficial use of this resource.

The goal of this project was to design, field test, and deploy a digital radio which uses the 220-222 MHz spectral allocation and is suitable for stationary point-to-point data communications applications. The target application for this project was the control (pan, tilt, and zoom) of a video camera located at the interchange of I-65 and the Borman Expressway. The wireless link extends from the camera location to the traffic operations center (approximately 1.5 miles). There were three main tasks needed to produce a deployable modem: 1) interface circuitry was required between the 220 MHz modem and the camera control keypad and the camera pan/tilt/zoom receiver, 2) the fabrication of a compact and rugged transmitter was required, and 3) the fabrication of a compact and rugged receiver was required. The receiver size constraints were more exacting than those of the transmitter as the receiver is deployed in a roadside cabinet, while the transmitter is deployed in the traffic management center. The work plan was divided into a set of twelve tasks.

The 220 MHz modem can serve INDOT as a general purpose link for low to medium rate data communications in a wide variety of applications. The most significant issue outstanding with regard to widespread implementation of the technology is the mass production cost and the availability of a reliable source of production versions of the device. Efforts are continuing at both Purdue and Ohio State toward further simplifications aimed at complexity reduction in the receiver. As topics for further study, the following should be considered: 1) a detailed cost/benefit analysis should be made comparing the 220 MHz technology to other alternative technologies, and 2) a preliminary design study of interoperability issues should be performed for the 220 MHz technology in transportation applications.

17. Key Words	18. Distribution Statement
wireless communications, ITS 220 MHz allocation, surveillance camera control, telemetry data transmission.	No restrictions. This document is available to the public through the National Technical Information Service, Springfield, VA 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	22	

Form DOT F 1700.7 (8-69)

Table of Contents

List of Figures

List of Tables

Abstract

The Federal Highway Administration has a nationwide allocation of five frequency pairs in the 220-222 MHz Narrowband Radio Services band which are intended for application in Intelligent Transportation Systems. These frequencies are available for use by state DOTs (subject to FHWA approval) and provide an attractive solution for certain low to medium bit rate data communications applications. However, given the limited bandwidth available in these channels, very efficient modems will be required to make maximum beneficial use of this resource.

The goal of this project is to design, field test, and deploy a digital radio which uses the 220-222 MHz spectral allocation and is suitable for stationary point-to-point data communications applications. The target application for this project is the control (pan, tilt, and zoom) of a video camera located at the interchange of I-65 and the Borman Expressway. The wireless link extends from the camera location to the traffic operations center (approximately 1.5 miles). There were three main tasks needed to produce a deployable modem: 1) the design of interface circuitry between the 220 MHz modem and the camera control keypad and the camera pan/tilt/zoom receiver, 2) the fabrication of a compact and rugged receiver. The receiver size constraints were more exacting than those of the transmitter as the receiver is deployed in a roadside cabinet while the transmitter is deployed in the traffic management center. The work plan was divided into a set of twelve tasks. The final task was the deployment of the unit on the Borman Expressway.

The 220 MHz modem can serve INDOT as a general-purpose link for low to medium rate data communications in a wide variety of applications. The most significant issue outstanding with regard to widespread implementation of the technology is the mass production cost and the availability of a reliable source of production versions of the device.

1 Introduction

Data communications systems linking field equipment (traffic sensors, changeable message signs, incident response vehicles, etc.) with traffic operations centers are a fundamental requirement of the Indiana Department of Transportation's (INDOT) plans for deployment of Intelligent Transportation System (ITS) traffic management and traveler information services. In 1992, five narrowband (4 kHz) frequency pairs in the 220-222 MHz Land Mobile radio band were allocated to the Federal Highway Administration (FHWA) for ITS applications. These frequencies are available for INDOT use (subject to FHWA approval) and provide an attractive solution for certain low to medium bit rate data communications applications. However, given the limited bandwidth available in these channels, very efficient modems are required to make maximum beneficial use of this resource.

The goal of this project was to design, field test, and deploy a digital radio which uses the 220-222 MHz spectral allocation and is suitable for stationary point-to-point data communications applications. The target application for this project is the control (pan, tilt, and zoom) of a video camera located at the interchange of I-65 and the Borman Expressway. The wireless link extends from the camera location to the traffic operations center (approximately 1.5 miles).

Some additional potential applications of this technology include: (1) data communications between highway infrastructure and mobile incident response vehicles, (2) transmission of surveillance sensor telemetry to remote concentrators, and (3) multiple access communications in semi-rural adaptive traffic signal coordination. Some aspects of these applications are the subject of further study.

2 Problem Statement

Given the limited bandwidth (4 KHz) available in the 220 MHz channels, very efficient modems will be required if profitable use is to be made of this resource. Standard twisted-pair telephone circuits also have an available bandwidth of about 4 KHz and modem technology has now evolved to the point where transmission rates are at 28.8 Kbps (or more) for the best twisted-pair lines. This amounts to a spectral efficiency of almost 9 bps/Hz.

The design of high efficiency wireless modems is more difficult than the design of wireline modems of similar efficiency because of challenging impairments present in a radio channel (fading, multipath, etc.). The Communication Research Laboratory at Purdue University has an ongoing research effort to optimize spectral efficiencies of wireless data transmission which has been used to leverage the work of the Borman Point-to-Point Modem Project. A wireless modem has been developed for fixed point-to-point one way data communication between the Borman expressway traffic management center (TMC) and a remote camera site located near the intersection of I-65 and the Borman Expressway. See Figure 1. The modem uses the ITS dedicated radio bands and provides 4800 bits per second of information throughput

and a range of more than 2 miles when properly installed. The modem will serve as the communication system for camera control functions.

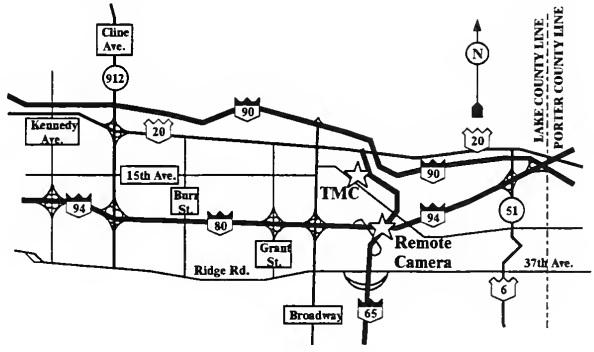


Figure 1: The vicinity of I-65 and the Borman Expressway interchange. White stars indicate the locations of the TMC and the camera. The point-to-point link of this project is line of sight between the two stars.

3 Objectives or Purpose

The majority of the effort on this project involved the development of a rugged compact implementation of the wireless modem. Significant research was also undertaken relating to this project under the auspices of an ITS-IDEA project funded by the Transportation Research board. The major design tasks undertaken in the INDOT funded work were:

- Design of Interfact Circuitry: The design of the electronic interface between the TMC communications controller and the wireless modem and between the modem and the video camera. This consisted of providing a transparent RS-422 standard interface as seen by the camera and camera controller.
- Transmitter Implementation: Fabrication of a compact transmitter which includes the interface circuitry, digital signal processor (DSP) modulator, the digital up converter, the radio frequency (RF) up converter and amplifiers, and the antenna systems.
- Receiver Implementation: Fabrication of a compact receiver unit which includes antenna system, the RF receiver, the sampler, the digital down converter, DSP demodulator, and interface circuits.

4 Work Plan

The work plan for this project was divided into a set of twelve tasks which are given in Table 1. The project experienced several long delays. The first delay involved Task 5 (RF System Design) and caused a project delay of approximately 8 months with respect to the original

schedule. The problem arose during acceptance testing of the RF subsystem which was designed and built by an outside contractor. The local oscillator in the RF unit (used in both transmitter and receiver) contained sufficient phase noise that the unit could not properly decode a multi-level constellation nor could it meet the regulatory transmission mask. The RF subsystem was redesigned and built by the Electro-Sciences Laboratory at the Ohio State University who were also responsible for the integration of the digital and RF circuits into a field deployable box.

Table 1: Status of Project Tasks.

PROJECT TASK	COMPLETION DATE	REMARKS
1. **Borman Expressway Requirements**	Feb. 1997	Produce specifications of interfaces between TMC and modem and between modem and camera controller.
2. **Interface Design**	June 1997	Design interfaces TMC/modem and modem/camera.
3. **Interface Acceptance Test**	August 1997	Test of interface designed in Task 2.
4. **Signal Design**	July 1997	Design signaling waveforms, coding, and frame structure for one-way point-to-point operation.
5. **RF System Design**	April 1998	Produce specifications for radio frequency (RF) subsystems, procure from subcontractor, and perform the acceptance test. This task required a second iteration as the first RF units did not pass the acceptance test.
6. **Demodulator Design**	August 1997	Design demodulator algorithms, DSP software, and printed circuit boards.
7. **Modulator Design**	August 1997	Develop DSP software to implement modulator algorithms.
8. **DSP Software Acceptance Test**	March 1998	Perform acceptance test of baseband modulator and demodulator software designed in tasks 6 and 7.
9. **Digital Hardware Acceptance Test**	June 1998	Perform acceptance test of all digital hardware systems.
10. **Integration and Test**	Dec. 1999	Perform acceptance tests on the entire system in the laboratory.
11. **Deployment**	April 2000	Deploy system on the Borman Expressway and perform acceptance tests on the deployed system.
12. **Final Report**	June 2000	

The second major delay occurred with the first attempt to perform Task 10 (Integration and Test) when the receiver unit failed its temperature test. Since the receiver must operate in a roadside cabinet which is not climate controlled, passing the temperature test was deemed essential. Various minor modifications were attempted by Electro-Sciences Lab personnel (enlargement of heat sinks, installation of a fan) though they did not solve the heating problem. Efforts to find a simple fix were exhausted in August 1999 when it was decided to procure a redesigned receiver (RF and digital circuitry) from Welkin Systems of San Diego, CA. The receiver unit was delivered to Ohio State in November 1999 and tested in December (Task 10). The complete Borman Point-to-Point Modem (including camera controller and pan/tilt/zoom receiver) was received at Purdue University in January 2000. Integration and test (Task 10) was repeated in the Communications Research Laboratory where all tests were passed. Deployment took place in April.

5 Analysis of Data

5.1 Design of the Interface Circuitry

The camera controller interface was designed for compatibility with the product by Kalatel which is in use on the Borman Expressway. The interface equipment consists of 1) a KTD-310 keypad which will reside in the TMC (this is the operator control keypad), and 2) a KTD-125 P/T/Z (pan/tilt/zoom) receiver which will reside in a roadside cabinet located next to the camera pole.

The design of the point-to-point modem is transparent to the data protocols used in the Kalatel system to control the camera functions. The only important point is that the interface between the two ends should satisfy the RS 422 standard (a balanced twisted pair physical connection). Thus the modem must provide a transmission function transparent to the Kalatel system. The interfaces are illustrated in Figure 2.

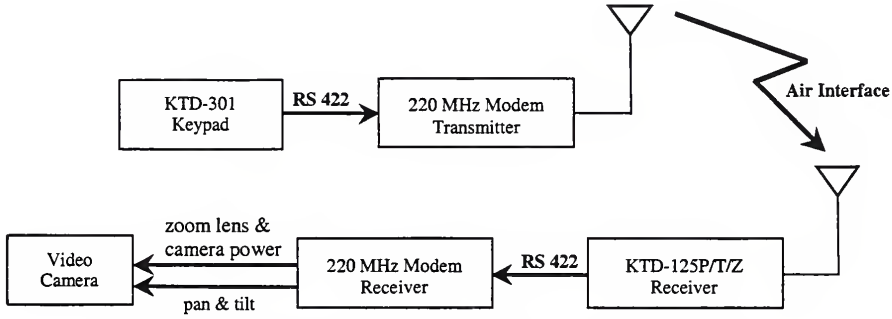


Figure 2: Illustration of modem and camera control interface.

5.2 Design of the Point-to-Point Modem

This portion of the project concerns the design of a high performance point-to-point data communication architecture. The point-to-point modem shares many architectural features with the mobile modem. The major difference is that the point-to-point modem does not require pilot symbol assisted modulation (PSAM) or diversity transmission. The work on this task has concentrated on the design of modulation and demodulation schemes optimized for point-to-point transmissions. A block diagram of the point-to-point transmitter and receiver is given in Figure 3.

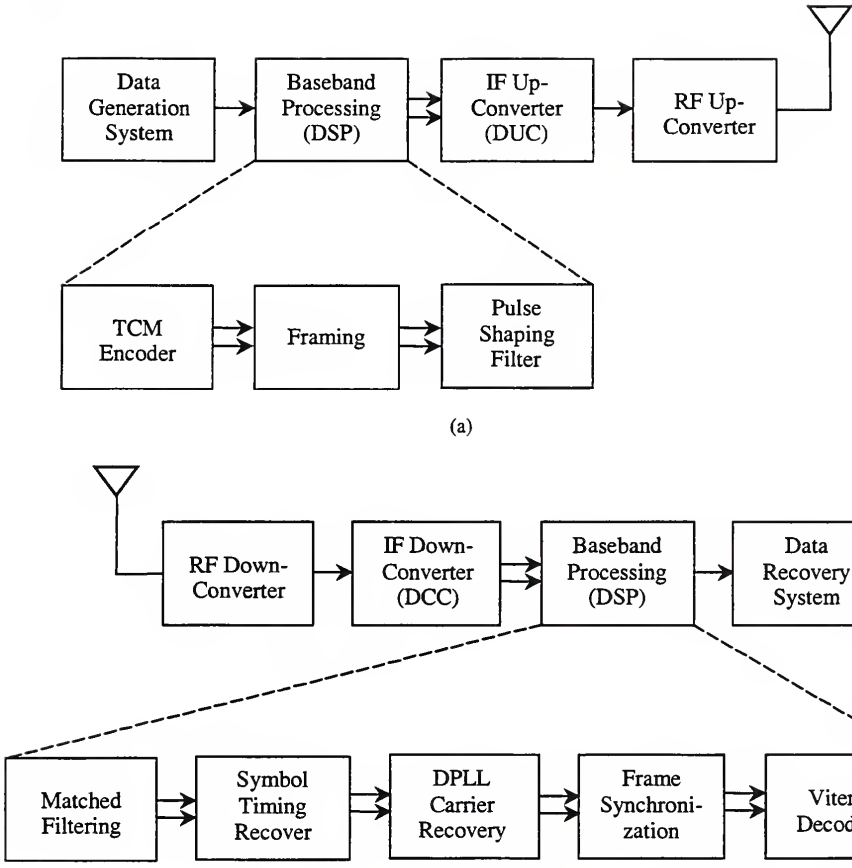


Figure 3: 220 MHz Modem Block Diagrams. (a) Transmitter. (b) Receiver.

The features of the point-to-point mode architecture include:

1. coherent demodulation via digital phase lock loop (DPLL) carrier recovery.
2. trellis coded modulation.
3. spectrally efficient pulse shaping and large QAM constellations (up to 128-QAM).
4. design to V.32 and V.33 wireline modem standards.
5. soft decision decoding.
6. linear high power amplifiers.

Further details of the point-to-point modem design may be found in [1] and in Appendix A.

5.3 Field Testing of the Point-to-Point Modem

The current implementation of the experimental system (the experimental system is not the same as the deployed system) uses a combination of hardware and software. The baseband modulator is implemented on a Motorola 56002 DSP. Samples are generated at a rate of 100 kHz. Using 28 samples per symbol period gives a symbol rate of 3571.4 Hz, the maximum that will fit in the FCC spectral mask. The baseband signal is sent to the Digital Up-Conversion (DUC) board which modulates the signal to an intermediate frequency (IF) of 21.4 MHz. Commercial off-the-shelf components are used the bring the signal up to a transmission frequency of 220.5825 MHz and to amplify it to 1/2 Watt. At the receiver the signal is amplified and down-converted to an IF of 10.7 MHz by an Analog Devices AD607 evaluation board. The IF signal is sampled at 40 MHz by the Harris HI5702 ADC and brought down to baseband by a Harris HSP50016 Digital Down-Converter (DDC). The DDC also decimates the sampling rate to 50 kHz. This sampled baseband signal is stored in the memory of a PC and then saved to a data file.

The remaining portion of the receiver and demodulator are implemented on the block-oriented software package, Signal Processing Worksystem (SPW). Although the final implementation uses a Analog Devices DSP for the demodulation, SPW was used for its versatility during the design phase.

Using the 4kHz channel bandwidth, the 3571.4 Hz symbol rate, and the synchronization sequence overhead, the bandwidth efficiencies can be calculated as 3.29 and 4.93 bps/Hz for the V.32 and V.33 modulation schemes, respectively. Field tests were conducted to observe the performance of this modem. Data was transmitted from the top of a parking garage in West Lafayette, IN near the Purdue University campus. The receiver was then used to collect the signal at a variety of locations throughout West Lafayette and Lafayette. Results generally fell into one of two categories. When the receiver did not have a direct line of sight with the transmitter, the resulting signal was not strong enough to demodulate (failure can be attributed to the DPLL). Although the DPLL performs in a reasonable fashion once lock has been achieved, its performance during acquisition is rather poor without high SNR.

When the receiver had a direct line of sight to the transmitter, performance was substantially better. Received signal constellations for the V.33 modem are shown in Figure 4 for transmission distances of 1.75 and 2.5 miles. In all V.33 cases, the BER was roughly 10^{-4} to 10^{-5} while V.32 transmissions gave no errors.

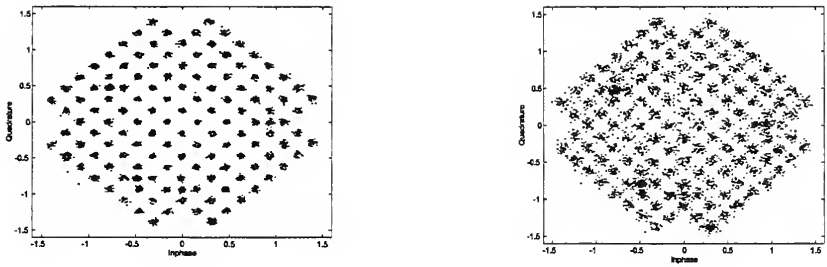


Figure 4: Received signal constellations from field testing. (a) Receiver located approximately 1.75 miles from transmitter. (b) Receiver located approximately 2.5 miles from transmitter.

5.4 Integrated Circuit Development

Communication system designs with large potential markets/production volumes can most effectively be implemented by using integrated circuit (IC) technology. IC technology is widely used in high performance consumer electronic devices like televisions, cellular telephones, and compact disk players. In a commercial endeavor, IC development is relatively expensive and labor intensive in terms of engineering time but the savings in production costs greatly outweigh this nonrecurring cost.

Figure 5 shows the block diagram for the receiver front-end. It is seen that the first three stages of the receiver are implemented with commercially available ICs. The fourth block (filtering and timing recovery) is currently implemented in software (SPW in the experimental modem and DSP code in the real-time modem). The same architecture for the timing recovery block can be used for both point-to-point and mobile applications and, moreover, this architecture will not change as more bandwidth efficient modulations and coding schemes are implemented. Also, by making several of the architecture's features programmable (e.g., filter tap coefficients) the IC will be useful in a wide variety of applications and would be an important component for a 220 MHz modem development.

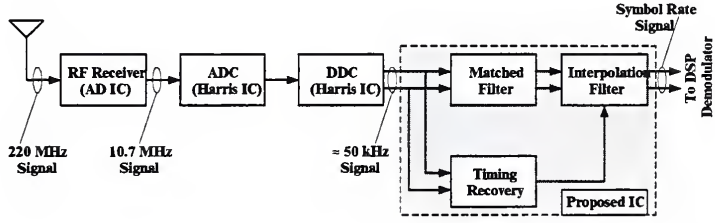
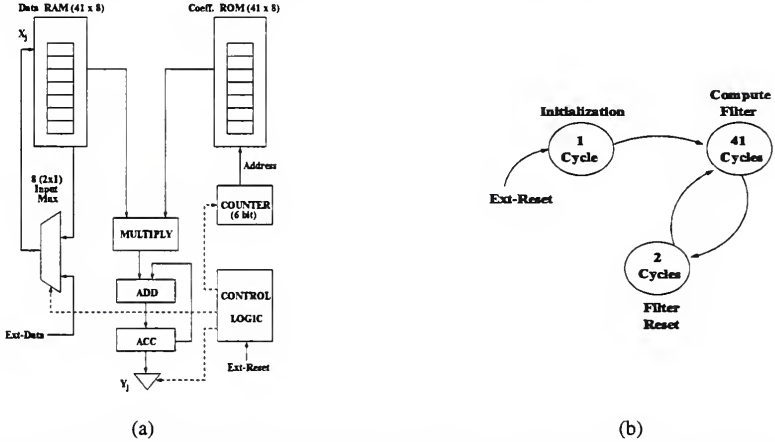


Figure 5: A block diagram of the ITS modem receiver and the proposed blocks to be incorporated in the IC development.

Motivated by the potential large scale production efficiency, an IC was designed for the symbol timing recovery functions of Figure 5. The implementation used standard CMOS library

cells in 1.2 μm technology, an 8-bit twos-complement architecture and a design emphasis based upon minimization of chip area. The transistor count of the final design was 148,000. The estimated chip area was 70 square millimeters and the estimated power consumption was 150 mW. The chip was not actually fabricated because the MOSIS fabrication costs ($36,000, 100 quantity, academic discount) were not included in the budget.

The majority of symbol timing recovery complexity (or chip area) is involved in the various finite impulse response filtering operations. The IC was designed so that the matched filter and prefilter shared the same architecture. The basic filter architecture is shown in Figure 6 including the multiply/accumulate unit and 3 state finite state machine controller.

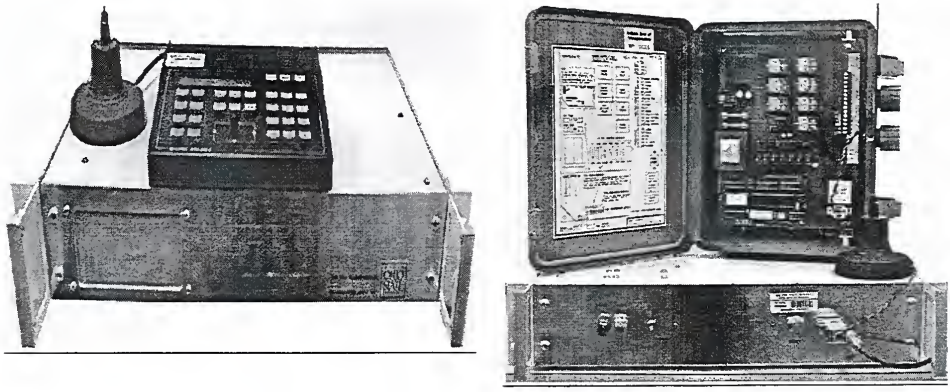


(a) (b)

Figure 6: Basic finite impulse response filter architecture used in symbol timing recovery integrated circuit design. The input sample rate is 15 kHz and the filter operates on a 645 kHz clock to compute one output in 43 cycles. (a) Multiply accumulate block. (b) Three state finite state machine controller.

5.5 Deployment and Test of the Borman Point-to-Point Modem

Hardware and software for a version of the modem design presented here were developed in cooperation with the Electro-Sciences Laboratory of the Ohio State University and Welkin Systems in San Diego, CA. The hardware was deployed in April 2000 in a camera control application in the vicinity of Interstate Highway 65 and the Borman Expressway (I-80/94). The link is line of sight of approximately 1.5 miles in distance. See the map of Figure 1. A closeup of the hardware in the laboratory is shown in Figure 7.

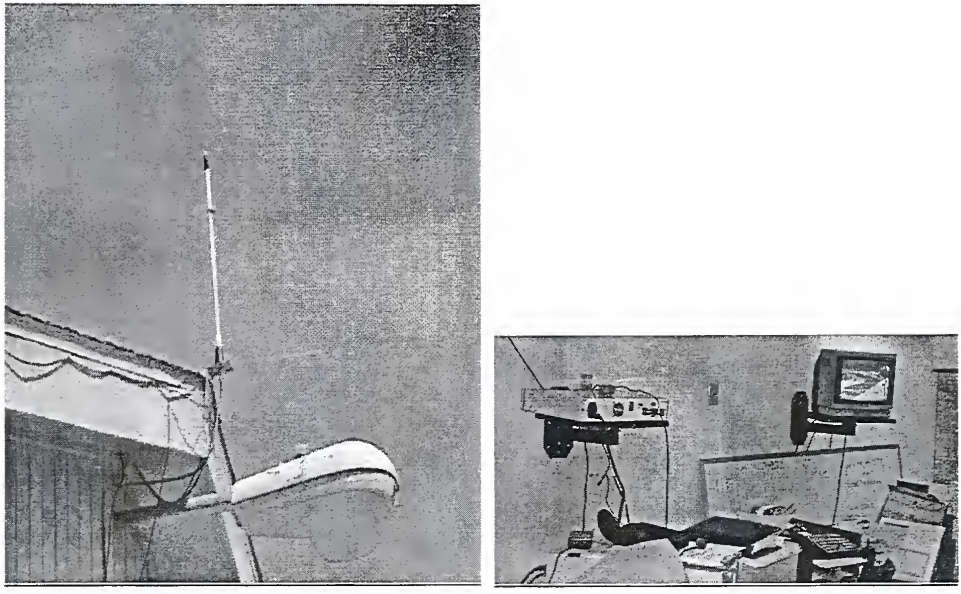


(a) (b)

Figure 7: Laboratory view of the Borman Point-to-Point Modem Hardware. (a) Transmitter built by the Electro-Sciences Laboratory of the Ohio State University. Shown on top of the transmitter box is the camera control operator's touch pad and joystick. (b) Receiver built by Welkin Systems. Shown on top of the receiver box is the camera control pan/tilt/zoom receiver.

Prior to deployment the hardware was tested in the Communications Research Laboratory and found to work according to the specifications for an extended period of time (approximately one week). Note that the real-time version of the hardware is not suitable for communications system tests of bit error rate or link availability as the required information is not logged. Such is outside the scope of the designed hardware.

The Borman Point-to-Point hardware was deployed in April 2000 at the INDOT Miller Unit (transmitter) and at the intersection of I-65 and the Borman Expressway (receiver). The radio link has functioned perfectly for approximately one month. Figure 8 shows the transmitter hardware and Figure 9 the receiver hardware.



(a) (b)

Figure 8: The Borman Point-to-Point Modem hardware deployed at the Miller Unit. (a) Transmitter antenna. (b) 220 MHz transmitter (at left) and video (at right) from the controlled camera.

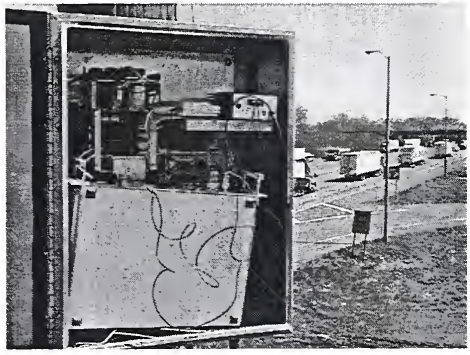


Figure 9: The Borman Point-to-Point Modem hardware deployed at the intersection of I-65 and the Borman Expressway (seen in the background).

6 Conclusions

This report has provided a detailed overview of the design of a point-to-point communications architecture based upon the 220 MHz ITS spectral allocations. The results presented herein are a

part of a larger project (funded in part by ITS-IDEA, Texas Instruments, and the National Science Foundation) that seeks to explore the limits of bandwidth efficiency in cellular stationary, mobile, and multiple access communications. The technical goals of spectral efficiencies of 3 bps/Hz for mobile operation and 5 bps/Hz for point-to-point operation have been met in field tests of the experimental SPW based modem. Effort continues to improve these spectral efficiencies further. In cooperation with the Electro-Sciences Laboratory at Ohio State University, transmitter and receiver hardware have been fabricated and deployed in a camera control function on the Borman Expressway.

7 Recommendations

The 220 MHz modem can serve INDOT as a general purpose link for low to medium rate data communications in a wide variety of applications. The most significant issue outstanding with regard to widespread implementation of the technology is the mass production cost and the availability of a reliable source of production versions of the device. Efforts are continuing at both Purdue and Ohio State toward further simplifications aimed at complexity reduction in the receiver. Regarding costs relative to other INDOT data communications alternatives and compatibility with existing equipment, the following tasks should be undertaken.

1. A cost/benefit analysis should be made comparing the 220 MHz technology to the following alternative communications technologies: (1) wireline connections through the public switched telephone network, (2) wireless connections using a cellular service provider, and (3) spread spectrum radios in the industrial-scientific-medical (ISM) bands. Where applicable the cost comparison should consider transportation related applications for medium bit rate data communications.

2. A preliminary design study of interoperability issues should be performed for the 220 MHz technology in transportation applications. In particular, the design requirements for 170/270 traffic signal controller backplane compatibility must be worked out.

8 Implementation Suggestions

This project has leveraged work funded by ITS-IDEA, Texas Instruments, and the National Science Foundation to produce a wireless communications resource for data communications on the Borman and other INDOT projects. The research has lead to a modem design optimized for multimode operation (stationary, mobile, and multiple access) with high bandwidth efficiency.

The communications architecture could be implemented to provide for multiple access communications in a local area network configuration as would be found in a sensor concentration application on the Borman Expressway. See Figure 10 for an illustration showing the sensor concentration scenario where traffic sensors are geographically distributed in a local area. Sensors in a cluster must be able to send their data to a local processor for preprocessing and concentration. Different types of sensors have different data communication requirements and sensors communicate asynchronously.

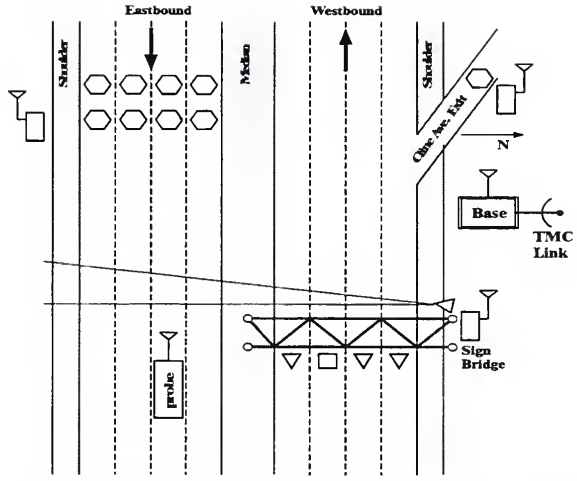


Figure 10: The sensor concentration scenario as might be implemented in a future Cline Avenue on the Borman Expressway.

9 References

1. M. J. Roos. Architectural design and implementation of a wireless narrowband fixed-point modem. Master's thesis, Purdue University, West Lafayette, IN, May 1997.

2. G. Ungerboeck and I. Csajka. On improving datalink performance by increasing the channel alphabet and introducing sequence coding. *In International Symposium on Information Theory,* June 1976.

3. G. Ungerboeck. Trellis-coded modulation with redundant signal sets, parts I and II. *IEEE Communications Magazine,* 25(2):5- 21, February 1987.

4. The International Telegraph and Telephone Consultative Committee. Data communication over the telephone network, series V recommendations, November 1988. CCITT Blue Book.

5. A. J. Viterbi. Error bounds for convolutional codes and an asymptotically optimum decoding algorithm. *IEEE Info. Theory,* IT 13:260-269, April 1967.

6. G. C. Clark and J. B. Cain. *Error-Correction Coding for Digital Communications.* Plenum Press, New York, 1981.

7. L. F. Wei. Rotationally invariant convolutional channel coding with expanded signal space Part 1. *IEEE Journal on Selected Areas in Communications,* SAC-2(5):661, September 1984.

8. M. K. Simon and J. G. Smith. Carrier synchronization and detection of QASK signal sets. *IEEE Trans. Commun.,* COM-22:98-106, February 1974.

9. A. Y. Chen, M. P. Fitz, and W. A. Sethares. A performance comparison of 16QAM digital PLL based demodulators. In *IEEE Globecom 1994,* pages 410-414, 1994.

10. F. M. Gardner. *Phaselock Techniques.* Wiley & Sons, New York, 2nd edition, 1979.

11. J. K. Cavers. An analysis of pilot symbol assisted modulation for Rayleigh faded channels. *IEEE Trans. Veh. Tech.,* vol. VT-40:686-693, November 1991.

12. L. E. Franks and J. P. Bubrouski. Statistical properties of timing jitter in pam timing recovery schemes. *IEEE Trans. on Commun.,* COM-22:913-920, July 1974.

13. A. N. D'Andrea, U. Mengali, and M. Moro. Nearly optimum prefiltering in clock recovery. *IEEE Trans. Commun.,* COM 34:1081-1088, November 1986.

14. M. Oerder and H. Meyr. Digital filter and square timing recovery. *IEEE Trans. Commun.,* COM 36:605-611, May 1988.

15. E. A. Lee and D. G. Messerschmitt. *Digital Communications.* Kluwer Academic Publishers, Boston, 1988.

16. J. P. Seymour. *Improved Synchronization in the Mobile Communications Environment.* Ph.D. thesis, Purdue University, West Lafayette, IN, 1994.

10 Appendices

Appendix A: The Design of the Point-to-Point Modem

A.1 Trellis Coded Modulation

Forward error control (FEC) coding is used to reduce the overall system bit error rate (BER) by adding a controlled redundancy to the transmitted signal. The point-to-point modem uses a combination of modulation and coding known as Trellis Coded Modulation (TCM). The technique, first introduced by Ungerboeck in 1976 [2], allows for significant coding gains while still maintaining bandwidth efficiency.

A.1.1 Encoding

In its most basic form, TCM may be viewed as performing two operations simultaneously. A block of κ bits is input to a convolutional encoder which outputs $\kappa+l$ bits dependent upon both the input bits and the previous state of the encoder. At the same time, the output bits are mapped to a signal constellation with an alphabet of $2^{\kappa+1}$ elements. The increase in alphabet size (by 2^l and the accompanying dependence on previous symbols are instrumental in making TCM an effective coding technique. The result is a "free distance" between coded symbol sequences that is significantly larger than the minimum Euclidean distance between uncoded symbols [3]. In point-to-point operation, the wireless modem can make use of the same TCM schemes used in wireline modems intended for use over the public switched telephone network. Two common trellis codes are defined in the CCITT V.32 and V.33 recommendations [4] which correspond to wireline data modems operating at 9.6 kbps and 14.4 kbps, respectively.

The convolutional encoder which corresponds to the V.32 recommendation is presented in Figure 11 and the trellis diagram is given in Figure 12. The mapping from the output of the convolutional encoder to the V.32 symbol constellation is shown in Figure 13. Similar diagrams for the V.33 recommendation may be found in [4].

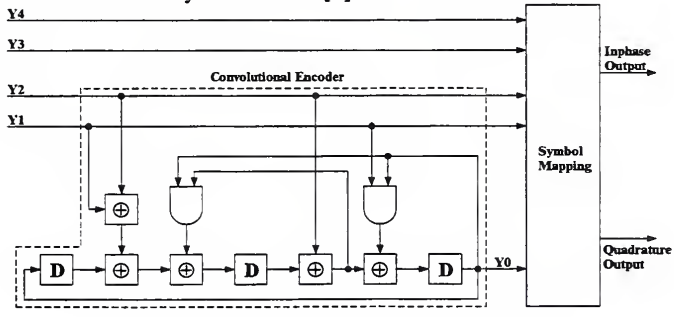


Figure 11: V.32 Convolution Encoder.

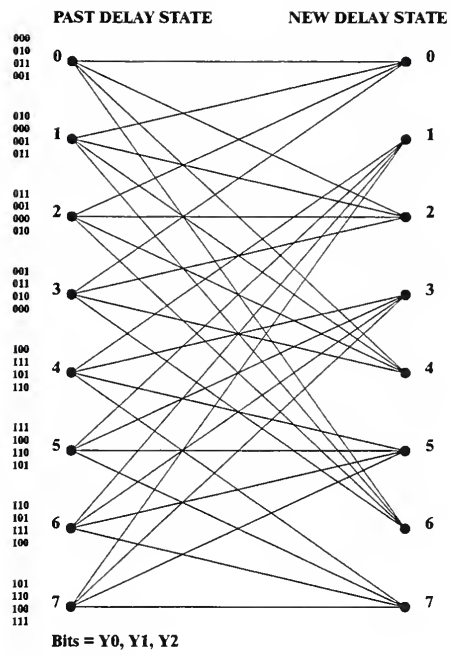


Figure 12: Trellis Diagram. The four groups of three bits next to each state in the trellis correspond to the four branches leaving the state.

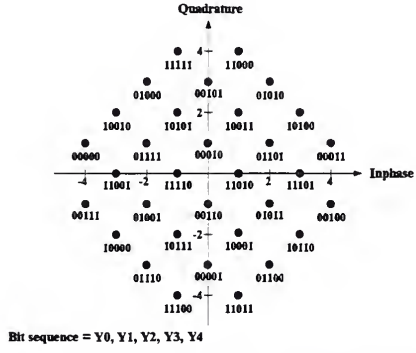


Figure 13: V.32 Constellation Point Mapping.

A.1.2 Decoding

A very efficient method of decoding the received noisy sequence employs the Viterbi algorithm. This decoder determines the most likely coded symbol sequence from the unquantized received sequence [5, 6]. For the decoder to be truly optimal it would need to have an infinite delay since any received symbol is dependent on all the symbols that come before it. However, it has been shown that near-optimum decoding is achieved by a decoder with a delay of four or five times the constraint length [6] which is equal to one plus the number of memory elements in the convolutional encoder. For example, the V.32 TCM has three memory elements so a near-optimum decoder would have a latency of $(3+1)\times 5 = 20$ symbol time periods. This number is also referred to as the truncation length, as paths through the trellis are truncated at this point and a decision is made.

The 220 MHz point-to-point modem architecture uses both the V.32 and V.33 recommendations for TCM. These architectures use convolutional encoders with a constraint length of four and thus a Viterbi decoding length of twenty is used for implementation. When used with a near-optimum decoder, these TCM schemes provide a coding gain of approximately 4 dB at high SNR [7]. Computer simulations were run using Signal Processing Worksystem (SPW), a block-oriented software package, to compare the uncoded and trellis-coded BER curves. Results are shown in Figure 14.

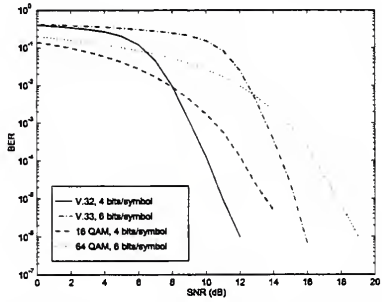


Figure 14: Uncoded and Trellis-Coded BER Curves.

A.1.3 Closing the Trellis

When using the TCM scheme the receiver must determine where the trellis coding begins in order to demodulate as effectively as possible. For this reason the data is not continuously coded and transmitted, but is instead separated into blocks and coded one block at a time. Each block of trellis-coded symbols is preceded by a unique sequence of symbols which can be used at the receiver to determine where each trellis-coded block begins and ends. Figure 15 shows a sequence of transmitted symbols. The symbols are lumped into frames of length N and each frame starts with a synchronization sequence of length L. Thus each N-length frame contains $N-L$ trellis-coded symbols which are to be demodulated by the Viterbi decoder in the receiver.

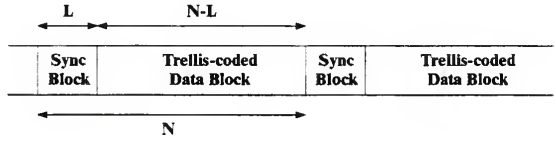


Figure 15: Transmitter Framing Scheme.

Details on the selection of the framing symbols and the method of synchronizing to them are found in [1]. The focus here is on the closing of each block of trellis-coded data. Recall that the decision on a received constellation point involves a sequence of points that immediately follow it. At the end of the trellis-coded block, future points cannot be used in the decision making process as coding has stopped for the insertion of a frame synchronization sequence. To assist in making good decisions at the end of the trellis-coded block, the encoder closes the trellis after all information bits have been coded. For example, once the last four data bits have been input to the TCM of Figure 11, the transmitter will send additional non-data related bits which will bring the encoder back to state zero. Note from Figure 12 that state zero can be reached from any other state in two transitions by taking the top branch from the previous state. Since each branch actually represents four parallel paths, the path corresponding to input bits $Y3=0$ and $Y4=0$ is used. This information is used in the Viterbi decoder of the receiver to aid in making a decision on the final points of the received trellis-coded block.

A.2 Carrier Recovery

After a signal is up-converted, transmitted, and down-converted, it is often recovered with a slight frequency offset due to the inaccuracies of various hardware oscillators. The received signal may be represented as

$$r(t) = m(t)e^{j(\Delta\omega t+\theta_0)} + n(t)$$

where $m(t)$ is the complex baseband signal, $n(t)$is complex white Gaussian noise, $\Delta\omega$ is the total frequency difference between the transmitter and receiver oscillators, and θ_0 is the initial phase offset. The frequency and phase offsets must be estimated and compensated for before

demodulation of the baseband signal can be done. This section provides the details of the digital phase-locked loop (DPLL) implemented in the point-to-point modem.

A.2.1 The DPLL of the Modem

The modem uses a decision-directed DPLL which operates on samples of the input signal taken at the symbol rate (see Figure 16). Although there are a number of different phase detectors that might be used, the one used here [8] has been shown to have better operating characteristics than several other common types of phase detectors used with QAM signals [9].

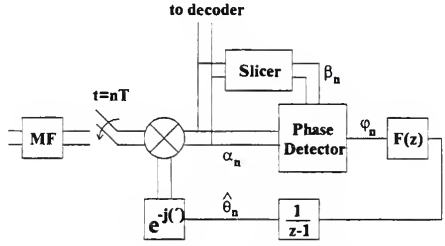


Figure 16: The Second-Order DPLL Used in the Modem.

The input signal is matched filtered, sampled at the symbol rate, T, and de-rotated by the current phase estimate. The de-rotated symbol, α_n, is input to the slicer whose output, β_n, is the data or synchronization symbol closest to α_n. The phase detector then calculates the angle between α_n and β_n, i.e.,

$$\phi_n = \arg(\alpha_n) - \arg(\beta_n)$$

$$\simeq \mathrm{Im}\{\alpha_n \beta_n^*\}$$

where the last equation is the implemented version. The phase error is sent through the loop filter, $F(z)$, and a discrete-time integrator with unit delay. This provides an estimate of the phase of the next symbol. The discrete-time integrator mimics the VCO of an analog PLL.

One way to characterize the performance of a phase detector is to plot its S-curve which is a plot of the true phase error versus the average detector output in the absence of noise. S-curves of the phase detector in Figure 16 are shown in Figures 17 and 18 for the V.32 and V.33 data constellations. Due to the $\pi/2$ symmetry of the constellations, the plots repeat themselves every $\pi/2$ radians.

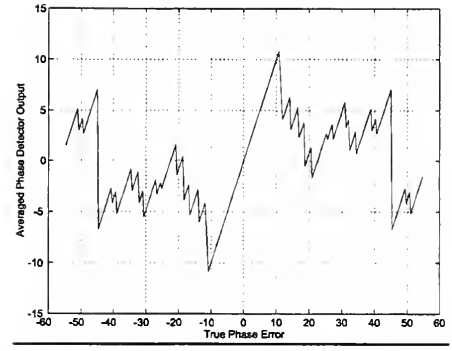


Figure 17: The S-curve for the Phase Detector of Figure 16 with a V.32 32-QAM Constellation.

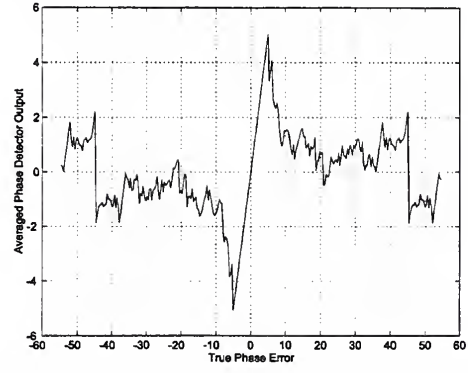


Figure 18: The S-curve for the Phase Detector of Figure 16 with a V.32 128-QAM Constellation.

In an ideal S-curve, the output of the phase detector would be equal to the true phase error. Unfortunately the phase detector under discussion will often give erroneous values due to false decisions by the slicer. However, it can be seen that when the true phase error is positive, the average phase detector output is nearly always positive as well, and likewise for a negative phase error. Thus even though the phase error provided by the detector is often incorrect, it will still guide the DPLL towards the true lock point. The only exceptions are a couple of false lock points in each of the plots. For example, in Figure 18 the detector output for a true phase error of 22° is zero. Recall however that this is the average of all possible phase detector outputs, and except for loops with a very narrow bandwidth, the DPLL phase estimate will move away from these points.

A.2.2 The Loop Filter

In order to lock onto a signal with both a phase offset and a frequency offset, a second-order DPLL must be used. Equivalently, a first-order filter of the form

$$F(z) = k_1 + \frac{k_2}{1 - z^{-1}}$$

must be used in the DPLL. The loop integrator, $G(z)$, combines with $F(z)$ to form a second-order filter. By making an analogy with the design for analog loops, we define

$$\begin{aligned} k_1 &= 1 - e^{2\omega_n T} \\ k_2 &= 1 - 2e^{2\zeta\omega_n T}\cos\left(\omega_n T\sqrt{1-\zeta^2}\right) + e^{2\zeta\omega_n T} \end{aligned}$$

where ζ is the damping factor and ω is the natural frequency [10]. In terms of these parameters the equivalent noise bandwidth of the loop is defined to be

$$B_{eq} = \frac{2(\alpha^2 + 2ab - 3)}{(\alpha^4 - 1) + 2(\alpha^2 - 1)ab} - 1$$

where

$$\begin{aligned} a &= e^{-2\zeta} \\ b &= \cos\left(\omega_n T\sqrt{1-\zeta^2}\right) \end{aligned}$$

In general, a larger B_{eq} allows the PLL to lock onto signals over a larger frequency range and to acquire a lock more quickly. A smaller B_{eq} provides better noise rejection and reduced transients during acquisition. The best design compromises between the two.

This information was used along with empirical observations to determine suitable gain parameters for the DPLL. In practice, it is common to design second-order loops with a damping factor of $\zeta = 1\sqrt{2}$ [10]. This practice was adopted to simplify the design of the filter since ω_n is then the only variable which needs to be specified. In fact, there are actually two values of ω_n that must be determined. The first is for use during the acquisition mode of the DPLL. It must be larger in order to accommodate a wide range of initial frequency offsets. The second is for use during the tracking mode of the DPLL. It must be smaller in order to reject noise and maintain a lower RMS phase error.

The design of the acquisition parameters relied heavily on empirical methods. It was found that using ω_n = 1000 radian/sec ($B_{eq} = 0.3388$) allowed for reasonable acquisition times for frequency offsets up to 5 percent of the symbol rate at a symbol SNR of 22 dB. Figure 19 shows curves of the average acquisition time over a range of frequency offsets. These curves were generated using computer simulations of the PLL/Frame Synchronizer system described in [1].

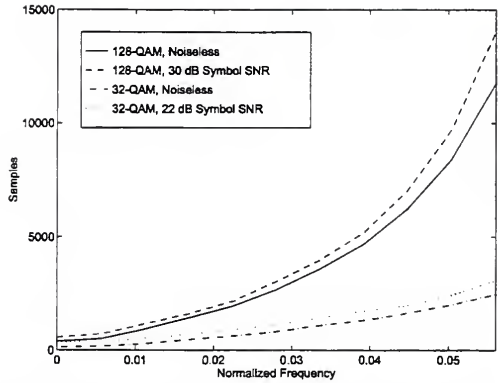


Figure 19: Average Acquisition Times of the DPLL.

In order to determine a reasonable value of ω_n for use during tracking mode, a few curves of the RMS frequency error were generated through computer simulations. Results are given in [1]. It was found that the RMS frequency error for the V.33 constellation increases rapidly as the normalized bandwidth exceeds 0.025. This effect occurs because the DPLL is not able to maintain a solid lock with a bandwidth this wide. The lower bound on the allowable bandwidth is dictated by the higher order characteristics of the signal phase. It was therefore decided to select a bandwidth well below the point where a lock could not be solidly maintained but large enough for the DPLL to compensate for time-varying frequency changes of the hardware implementation. The natural frequency was chosen to be ω_n = 25 radians/sec which corresponds to a bandwidth of B_{eq} = 0.0075.

As previously mentioned, it is common for a DPLL to have a bandwidth which adjusts to the state of loop. A wider bandwidth is desired during the acquisition mode so that a wide range of frequency offsets can be estimated and a narrower bandwidth is desired during the tracking mode to reject noise and maintain a solid lock. In order to implement a DPLL such as this it is necessary to determine when lock has occurred and how to adjust the bandwidth. A obvious solution for this problem which requires little increase in complexity is to use feedback from the frame synchronizer. The frame synchronization feedback is described in more detail in [1].

In order to compare performance of the full system to the curves of Figure 14, computer simulations were run. Figure 20 shows the results. This data was taken once the system had reached a steady-state, i.e., bit errors which occurred during the DPLL and frame synchronizer acquisition stages are not included. Notice that no data was taken at very low SNR. Once the SNR drops below a certain threshold, the DPLL can no longer maintain a solid lock on the signal constellation. This is not of great concern however, since these SNRs also correspond to bit error rates which are too low to be used in practice.

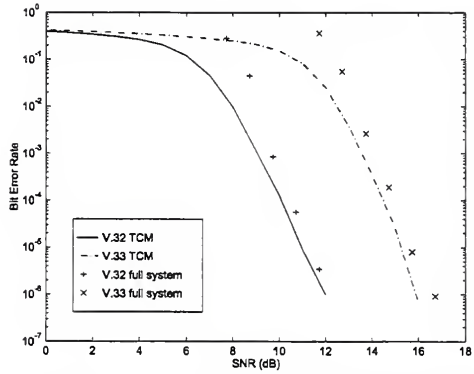


Figure 20: Steady-state BER curves of the modem.

Appendix B: Real Time Implementation of a Symbol Timing Recovery

B.1 Introduction

The goal of high bandwidth efficiency in wireless data transmission is often met by using large signal constellations, trellis coded modulations, and transmitted references for coherent detection [11]. However, the use of more sophisticated modulation places increasingly stringent requirements on the synchronization systems in the receiver including the symbol timing recovery which is performed at the first stage of the baseband receiver. For satisfactory performance in modulations with large constellations (e.g., 64- and 128-QAM), timing uncertainty must be held to a very small fraction of the signaling interval in order to attain satisfactory performance.

If the received signal has a discrete spectral component at a harmonic of the symbol frequency, the symbol timing algorithm may be as simple as a filter tuned to this harmonic. However, most situations require that the transmission of such spectral components be avoided. In a practical transmission scheme, a discrete spectral component can be produced by inserting a non-linear element before the tuned filter in the timing recovery circuit. This ad-hoc timing recovery method is known as the filter and square algorithm in the literature [12, 13, 14]. Timing jitter is caused by the combined action of thermal noise and the random nature of the transmitted data. At reasonably high signal-to-noise ratio (SNR), performance is therefore limited by the data dependent jitter which is strongly influenced by the shape of the data pulse at the input to the nonlinear element.

Digital realizations of receivers for synchronous data transmission are of growing importance as the capabilities of digital signal processors increase. To take advantage of this trend as much of the receiver function as possible should be should be digital. In other words,

the input signal should be sampled by a free running oscillator and all subsequent receiver processing should be done in discrete time on the samples.

B.2 The Symbol Timing Architecture

The symbol timing estimator and matched filter architecture is shown in Figure 21. The input to the matched filter consists of samples of the noncoherent in-phase and quadrature channels of the received baseband signal $r(t)$. The sampling rate $1/T_s$ is chosen as a multiple N_s of the symbol rate $1/T$. The objective of the timing estimator is to determine the optimal point to sample the output of the matched filter as shown in the figure. Not only is there an unknown time delay between transmitter and receiver but also the transmit and receive clocks are not synchronous. Thus the optimum matched filter sample time will drift. The timing estimation algorithm must be able to track this. The delay block in Figure 21 is used to compensate for additional delay introduced by the timing estimation algorithm itself.

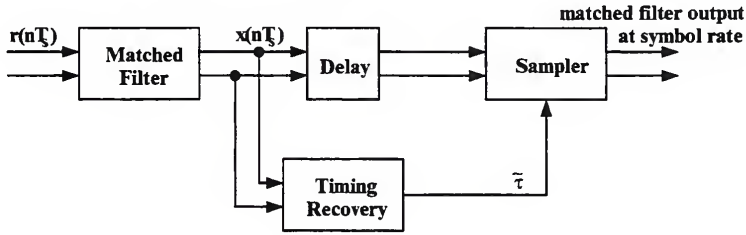


Figure 21: Matched filter and recovery algorithm.

The architecture of the timing estimator is shown in Figure 22. The timing estimator is based upon the filter and square algorithm [12, 13]. The algorithm extracts a timing waveform $z(nT_s)$ whose zero crossings correspond to the optimal sampling instants for the matched filter output. More detail on the subblocks in the algorithm are presented below.

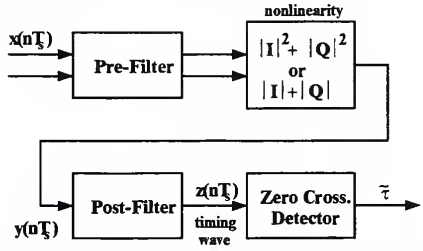


Figure 22: Architecture of timing estimation block.

B.2.1 The Prefilter

Franks and Bubrouski [12] have shown that by using the appropriate prefilter with the magnitude squared nonlinearity the data dependent noise is entirely eliminated. The requirements are:

1. prefiltered pulses have conjugate symmetry about the frequency $2/T$ and are bandlimited to $1/4T \leq |f| \leq 3/4T$, and
2. the transfer function of the postfilter has conjugate symmetry about the symbol rate $1/T$ and a bandwidth less than $1/T$.

Denoting the square-root Nyquist pulse shape $p(t)$, a simple discrete time prefilter that will meet these conditions is

$$h(nT_s) = \cos(2\pi nT_s / T)\, p(nT_s) * p(-nT_s)$$

This is simply the Nyquist pulse modulated in frequency to the symbol rate. Other researchers have derived similar constraints for other nonlinearities [13].

B.2.2 The Nonlinearity

Various authors have noted that other nonlinearities such as magnitude, magnitude to the fourth power, etc., provide better performance in some cases. Lee and Messerschmitt [15] have suggested that the magnitude nonlinearity gives better performance for high order quadrature amplitude modulation (QAM) constellations.

B.2.3 The Postfilter

Three possibilities for the postfilter are: an infinite impulse response (IIR) filter, a finite impulse response (FIR) filter, or a phase locked loop (PLL). While the IIR filter is attractive for its low complexity, it is not acceptable for timing recovery because it does not have linear phase. The drawback of an FIR implementation of the postfilter is that a prohibitively large number of taps would be required to provide an adequately narrow bandwidth.

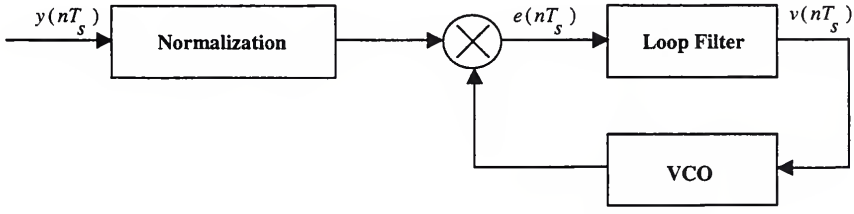


Figure 23: Digital phase locked loop as postfilter.

A PLL can meet both performance and complexity requirements in the postfilter application (see Figure 23). An input normalization is required to insure that the PLL receives a signal with constant power. One possibility for normalization is to subtract the sample mean and

divide by the sample standard deviation. A less computationally complex normalization would consist of a mean normalization followed by a hard limiter.

The loop filter is the following first order IIR filter:

$$v(nT_s) = v((n-1)T_s) + e(nT_s) - \alpha e((n-1)T_s)$$

where

$$\begin{aligned} \alpha &= (1 - e^{-4\zeta\pi f_n T_s}) / k \\ k &= 2(1 - e^{-\zeta 2\pi f_n T_s} \cos(2\pi f_n T_s \sqrt{1-\zeta^2})) \end{aligned}$$

The PLL damping factor ζ and the undamped natural frequency f_n have been chosen to be ζ = 0.9 and f_n = 5 Hz. The modem operates at a symbol rate of 3570 Hz using a square-root raised cosine pulse shape with roll-off β=0.15. The timing waveform $z(nT_s)$ is the output of the voltage controlled oscillator (VCO) in Figure 23.

B.2.4 The Sampler

It is unlikely that the timing estimate will coincide with one of the digital samples, so the sampler needs to interpolate between the nearest two samples. Ideal interpolation requires many clock cycles; if the number of samples per symbol (N_s) is sufficiently large a linear or quadratic interpolator will be adequate.

B.3 Complexity Considerations in DSP Implementation

B.3.1 Hardware Design

The system is implemented on a TI TMS320C541 16 bit fixed point DSP which has 5k of on-chip RAM and an 80 Mhz clock rate. A combination of C and assembly code is used in the implementation. The C54x allows treatment of non-integer numbers as fractions simply by setting a register flag. We use a combination of C and assembly code in the implementation. The experimental system uses a personal computer (PC) as the interface between an intermediate frequency to baseband digital down conversion (DDC) board and the DSP evaluation board. An application has been written which reads data from the DDC board, passes it to the DSP board, waits until DSP processing for that data set is finished, and then reads it back to save it into a file. The data passed between the DDC and the DSP consists of 8-bit in-phase and 8-bit quadrature samples.

B.3.2 Complexity Estimation

The estimation of the number of operations needed to process data is presented in Tables 2 and 3. Estimated memory requirements are given in Table 4. The TI C54x DSP can do multiplication, addition, and calculation of circular array index in 1 cycle, which significantly improves processing speed.

Table 2: Estimated Computational Complexity.

Subsystem	Cost	Operation
I/O	2	Read/write I/0
Matched Filter	$2(N_s N_w + 1)$	Read/write/I/0
Prefilter	$2(N_s N_{wp} + 1)$	MAC
Nonlinearity	2	absolute value
	1	add
PLL Normalization (Hard limiter)	N_s	add
	1	divide
	1	branch test
PLL	4	multiply
	3	add/subtract
	1	sine lookup
Zero Crossing	$2N_s$	branch tests
	1	branch tests
	1	divide
	2	add/subtract
Interpolator	1	multiply
	2	add/subtract

Table 3: Estimated Total Complexity on C54x.

Operation	Total Cost	Cycles per instruction
sine lookup	1	2
divide	4	22
MAC	$2N_s(N_w - N_{wp} + 2)$	1
square	1	1
multiply	5	1
add/subtract	12	1
absolute value	1	1
branch tests	$2N_s$	5
read/write I/0	2	20

Table 4: Estimated Memory Requirements.

Subsystem	Memory
Matched Filter	$N_s N_w + 1$
Prefilter	$N_s N_{wp} + 1$
Delay	$N_s N_{wp}$
PLL Normalization	2
PLL	4

B.3.3 Complexity Reduction

Implementation of the variance normalization in the PLL subsystem would take 3 divide operations and a square root. A simpler normalization consisting of a mean correction followed by thresholding was chosen. There was no significant performance penalty paid for the simplification.

An attractive alternative to the magnitude squared nonlinearity is to add the absolute values of the in-phase and quadrature components. Not only does this require less clock cycles, but it also requires less dynamic range which is an important issue for fixed point DSPs.

QAM requires the system to have linear phase, so an FIR square-root raised cosine filter was chosen for the Nyquist pulse shape. The pulse was truncated at N_w symbol periods left and right of the origin giving a total of $N_s N_w$ filter coefficients. If N_s is too small the interpolation operation of the sampler will induce too much intersymbol interference (ISI), and if N_w is too small the pulse shape will no longer meet the Nyquist criterion.

B.4 Illustration of Complexity/Performance Tradeoffs

The timing recovery subsystem was implemented in the Signal Processing Worksystem (SPW) to quantify tradeoffs between complexity and performance. Simulations demonstrated that for all scenarios tested there was negligible loss in bit error probability (BEP) performance when using the absolute value nonlinearity in place of the magnitude squared nonlinearity, and negligible loss when using 4 samples per symbol. Furthermore, using the hard limiter to normalize the input to the DPLL did not degrade performance noticeably.

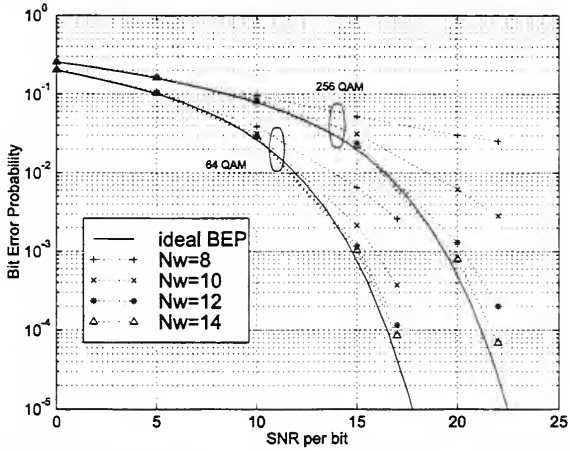


Figure 24: BEP for DFS timing recovery, 64 and 256 QAM in AWGN, $N_s = 4$ absolute value nonlinearity, and hard limiter PLL normalization.

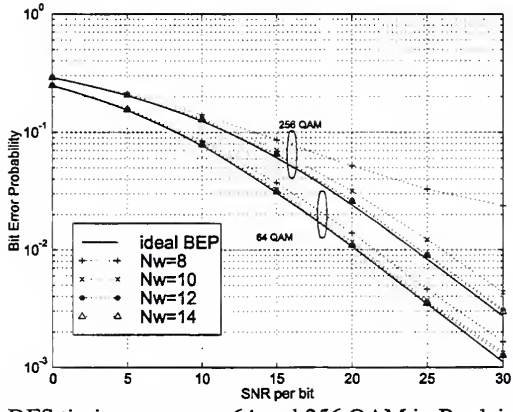


Figure 25: BEP for DFS timing recovery, 64 and 256 QAM in Rayleigh fading, $N_s = 4$, absolute value nonlinearity, and hard limiter PLL normalization.

BEP curves for uncoded QAM are shown in Figures 24 and 25 along with the analytical BEP. The gray bit mapping from [16] was used to facilitate calculation of the exact analytic BEP. The result in Figure 25 is for slow varying, frequency non-selective Rayleigh fading with ideal channel state information (CSI).

Several observations may be made from these BEP plots. Truncating the matched filter to $N_w = 12$ symbol periods (6 on either side of the origin) causes tolerable degradation in BEP and results in a FIR filter length of 49 samples. Using $N_w = 14$ is closer to ideal performance and only costs 8 more coefficients. Note that in fading the BEP when $N_w = 8$ levels off at high SNR - if the ISI induced by filter truncation is too severe, bit errors will result even when SNR is extremely high. Figure 26 shows the effect of truncation length on the signal constellation.

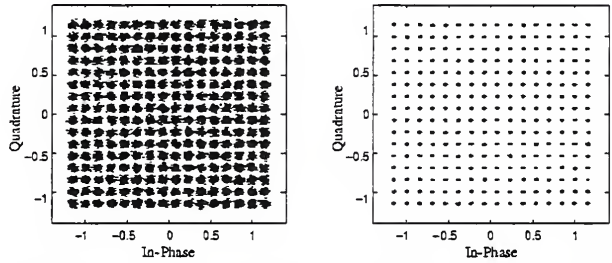


Figure 26: QAM scatter plots in the presence of no AWGN. Left $N_w = 10$, right $N_w = 14$.

Appendix C: Borman Wireless MODEM Operator's Manual

Ver 1.0 (updated), Author: Zhilin Liu, IPS Wireless Communications Laboratory, Department of Electrical Engineering, The Ohio State University, Nov. 1999

C.1 Introduction

Borman wireless MODEM is for ITS (Intelligent Transportation System) applications. The Borman Modem is made up of a transmitter unit and a receiver unit. The radio uses narrow-band (<4KHz) data communication with center carrier frequency of 220.5625MHz. Both the symbol rate and bit rate for the delivered radio are 3.2kHz as the modem uses one bit/symbol trellis coded QPSK modulation.

This manual describes how to operate Borman MODEM, especially how to hookup the system and troubleshoot it quickly. The basic system consists of a transmitter, a receiver, an input keypad and a camera controller.

C.2 Overview of the Modem System

C.2.1 Interface and Protocol

This Modem system has a maximum throughput of 3.2K bits/second. The radio transmitter uses an RS-422 2-wire serial interface for data reception only. The protocol uses a format of 2400bps, 8 data bits, 1 stop bit, and no parity. The radio receiver uses both RS-232 interface and protocol for data transmission. The format of the RS-232 transmission protocol is also 2400bps, 8 data bits, 1 stop bit, and no parity. Note that an RS-422 receiver is capable of receiving an RS-232 transmission, since RS-232 uses negative logic and signals are carried as single voltages referred to a common earth, wherein –3~-15v is 1(high level), +3~+15v is 0 (low level), and RS-422 uses balanced transmission, where Posi. – Nega.> +0.2v is 1, Posi. – Nega. < -0.2v is 0. The detailed interface information is given below.

C.2.2 Transmitter Unit

The transmitter unit accepts information bits through RS-422 serial interface from the outer terminal (such as input keypad) and transmits this information over a radio frequency carrier of 220.5625MHz. The transmitter unit has a front view shown in Figure 27. The left rectangle is a window through which you can see two LED lights. When they are lit, power is on and the transmitter is working.

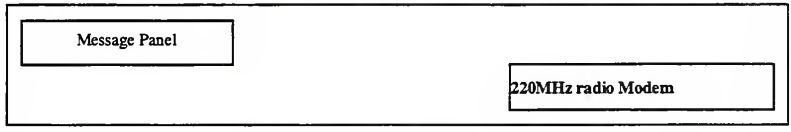


Figure 27: Transmitter front panel.

The main connections of the transmitter are situated at the back panel. They are as shown in Figure 2. The important connection details in Figure 28 are given as

1. Power switch,
2. Power input,
3. Fan,
4. Reset button,
5. RF output (antenna) (N Connector),
6. Wiring terminals.

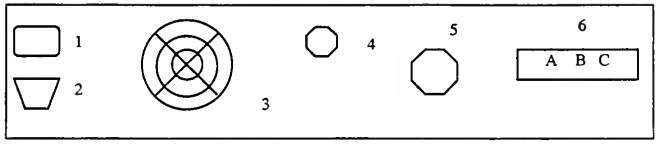


Figure 28: Transmitter back panel.

The wiring terminals (6) are for an RS-422 2-wire serial interface. Only the two left most terminals are used (**A: +** and **B: --**). The terminal A is connected to the positive end of RS-422, and terminal B is connected to the negative end of RS-422.

C.2.3 Receiver Unit

The receiver has a front panel as shown in Figure 29

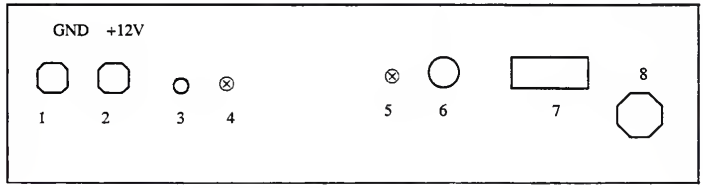


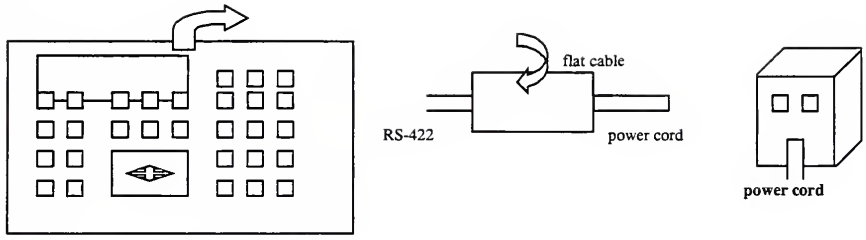
Figure 29: Receiver front panel.

The important connection details in Figure 29 are given as

1. GND,
2. +12V (@1.5A),
3. Power switch,
4. Power indicator (LED),
5. Sync indicator (LED),
6. Reset button,
7. DB-9 Female serial socket,
8. RF input (antenna) (TNC connector).

C.2.4 Accessories

The accessories consist of the **input keypad**, **camera controller**, **2-wire-to-DB-9 converter**, **DB-9-to-2-wire converter** and a **single 12V DC power supplies** with rated output current of 1.5A (not included). The keypad is used to input user's command and control remote camera. It has a control panel as shown in Figure 30(a), a connection box as shown in Figure 30(b), and an AC/DC adapter as shown in Figure 30(c).



(a) input keypad panel (b) keypad connection box (c) AC/DC adapter

Figure 30: Input keypad.

The RS-422 2-wire serial lines in Figure 30(b) are to be connected to the rear panel of the transmitter as described in Section C.3.

The **camera controller** is basically a black box, which controls the camera. The guide for its internal setting is posted under the top lid. It has a power cord which is to be plugged into 110V AC socket, and a RS-422 2-wire DB-9 male plug, which is connected to DB-9 female serial socket on the front panel of the transmitter.

The **2-wire-to-DB-9 converter** is used to convert the 2-wire DB-9 plug of the camera controller to real 2-wire so that it can be directly connected to the input keypad (with 2-wire output) and work in the wired mode (for test purpose, see Section 4). The wiring inside the plug is: Black (positive end of RS-422)—Pin 5(GND), Red (negative end of RS-422)— Pin 2(TX, from the point of view of the receiver).

The **DB-9-to-2-wire converter** is used for the interface of DB-9 RS-232 (which is widely used on PC) with RS-422 (which is the input configuration of the transmitter). The wiring inside the plug is: Pin 3 (TX, from the point of view of PC) — Red (negative end of RS-422), Pin 2 (RX) — NC (not connected), Pin 5 (GND) — Black (positive end of RS-422), Pin 7 (RTS) — 8 (CTS), Pin 6 (DTS) — Pin 4 (DSR) — Pin 1 (DCD). So this converter just supports unidirectional data flow from RS-232 → RS-422.

The **single 12V DC power supplies** should be able to provide 1.5A output current. It is connected to the power input terminals (1 and 2 in Figure 29) of the transmitter.

C.3 Equipment Setup

C.3.1 Radio Transmitter

Before beginning ensure that the transmitter power switch is in the off position.

C.3.1.1 Connect an **information source** which supports RS-422 to terminal A and B of the transmitter wiring terminals. See Section C.2.2 for connection details. Make sure RS-422 interface is operating.

C.3.1.2 Connect the antenna to the RF output port.

C.3.1.3 Plug the AC power to the back panel of TX.

C.3.1.4 Turn on the power switch on the back panel of the TX.

Now you can see the two LED lights on (one is red, one is green) through the window on the front panel of the TX. It indicates the transmitter is working.

C.3.2 Radio Receiver

Before starting ensure the receiver is in the power-off state.

C.3.2.1 Connect the outer terminal (**information sink**) to DB-9 female serial socket on the front panel of the RX. Since the RX uses RS-232 as its output interface, you can connect the terminal with RX directly if the terminal also uses RS-232 interface (PC is an example). If the terminal uses RS-422 interface, just connect DB-9's Pin 2(TX) to the negative (Red) end of RS-422 and Pin 5 to the positive (Black) end of RS-422. For the camera controller, this connection is already done, so just connect the DB-9 male plug of camera controller to the DB-9 female socket directly.

C.3.2.2 Connect the antenna to the RF input port.

C.3.2.3 Connect the output plugs of the DC power supplies (12V/GND@1.5A) to the power socket on the front panel of the RX (see (1), (2) in Figure 29)

C.3.2.4 Turn on the power switches both on the DC power supplies and on the RX.

C.4 Troubleshooting

C.4.1 Normal Mode of Operation

If you follow the procedures described in Section C.3, your Modem system should be easily setup and work normally. When the LED light is seen on through the message window on the front panel of the transmitter, the transmitter is working. When the **Sync light** (LED) is lit on the front panel of the receiver, it shows the receiver has acquired correct synchronization and works well. So, the information source and the information sink can communicate data normally.

The transmitter should be outputting at least 10dBm of RF power. The whole modem system should support a maximum path loss of 120dB. When SNR =12dB, less than 10^{-7} bit error rate should be achieved.

C.4.2 Troubleshooting Tips

In case your system doesn't seem to be working normally, try the following tips.

C.4.2.1 *The LED light is off as seen through the message window on the front panel of the transmitter?*

Check the power cord connection of the transmitter and that the power switch is in the on position.

C.4.2.2 *The power indicator (LED) on the front panel of the receiver is off?*

Check the connection between the DC power supplies and receiver. Additionally, check the switches on the power supplies and receiver.

C.4.2.3 *Sync light on the front panel of the receiver is off?*

First make sure the power indicators both on the transmitter and receiver are on according to C.4.2.1 and C.4.2.2. Then check the antenna connections of both the transmitter and receiver are tight.

If the Sync light is off then the receiver cannot acquire correct synchronization from the received signal. The problem may involve the transmitter, receiver and the radio channel as a whole. In some situations, the signal to noise ratio (SNR) is low, the Sync light intermittently turns off. This behavior is normal. If the Sync light stays off for a long time and the SNR is reasonably high, pushing the RESET button(s) on the receiver or/and the transmitter once to let the receiver or/and the transmitter restart may fix the problem. Reset the receiver first, and if that doesn't help, then try resetting the transmitter.

C.4.2.4 *The received data is garbled?*

First make sure the Sync light on the front panel of the receiver is on. The garbled data is generally due to a large interference in the radio environment. The interference from other equipment working in the same frequency band is very pernicious and it can even disrupt the operation of the Modem system totally. Try to avoid using two same frequency transmitters simultaneously in the same small area.

If all the indicators (including the power indicators and Sync indicator) are lit, all the connections are tight enough, and there is also no evident interference existing, but the system still produces garbled data, try pushing the RESET button(s) on the receiver or/and the transmitter.

C.5 Addenda

C.5.1 Wired Test Mode for the Keypad and Camera Controller

To get the camera controller working in the wired mode, connect directly the red and black wires of the keypad and the camera controller (via **2-wire-to-DB-9 converter**). From the keypad, set the camera number from 01 to 01. Then push the joystick around in different directions to hear different relays clicking. Most of the other keys on the keypad don't seem to produce any relay-clicking response.

* Note: There are some switches in the controller box that can be set to 0 or 1 and this determines the camera controller's number. The current setting is 01.